REMARKS/AGRUMENTS

Reconsideration of this application, as amended, is respectfully requested. The following remarks are responsive to the Office Action mailed February 24, 2004.

Corrected formal drawings are submitted, herewith.

Claims 1-42 are pending.

Claims 1-42 stand rejected.

Claims 1, 15, and 29 have been amended. It is respectfully submitted that no new matter has been added.

Claims 1-42 are rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,110,217 of Kazmierski, et al., (hereafter, "Kazmierski") in view of U.S. Patent No. 5,880,959 of Shah, et al., (hereafter, "Shah") and U.S. Patent No. 5,933,345 of Martin, et al., (hereafter, "Martin"), individually.

DRAWINGS

Applicants submit corrected formal drawings herewith.

CLAIM REJECTIONS – 35 USC §103 (a)

The Examiner rejected claims 1-42 under 35 U.S.C. §103(a) as being unpatentable over Kazmierski. Applicants submit that claims 1-42 are not unpatentable over Kazmierski in view of either Shah, or Martin. In regard to the rejection of claim 1, the Examiner has stated in part that:

> Kazmierski et al. (217) teaches:...configuring said blocks in a block diagram structure; (col. 4, lines 34 et seq.) ordering said blocks in said block diagram structure to allow for waveform relaxation of sets of variables of said blocks; and performing waveform relaxation of said sets of variables of said blocks. (Office Action, 2/24/04, p. 4)

Applicant respectfully submits that claim 1is not made obvious by Kazmierski in view of either Shah or Martin. Claim 1 recites the features of "*mixing a reference input signal and an error signal to generate non-relaxed variables, converting the non-relaxed variables into input relaxation variables through waveform relaxation, processing the input relaxation variables with a high fidelity plant model, generating non-relaxed output variables with the high fidelity plant model, converting the non-relaxed output variables into output relaxation variables through waveform relaxation, and providing the output relaxation variables to a low order controller that generates the error signal*". (Emphasis added) These features are not disclosed by Kazmierski as shown by the following analysis. Kazmierski describes a system and method for synchronization of multiple analog servers on a simulation back plane. (Kazmierski, title) More specifically, Kazmierski simulates electrical circuits that are divided into sections. Each section has a section specific simulator module associated with it. The simulation modules communicate using block waveform relaxation. (Kazmierski, abstract) Kazmierski runs a simulation in which waveforms are received as inputs and outputs are generated by the circuit simulator. (Kazmierski, col. 5, ll. 28-58) It is unclear if and how Kazmierski uses waveform relaxation with his circuit simulator. Regardless, Kazmierski describes the use of circuit design simulation tools and not a controller of a system for manufacturing. Because of this inherent difference, Kazmierski describes neither a high fidelity plant, input relaxation variables, output relaxation variables, nor a low order controller.

Nor does Martin describe the above-identified features of claim 1. Martin describes a method and apparatus for dynamic and steady state modeling over a desired path between two end points. (Martin, title) Although Martin discloses the use of a plant, and various controllers for such plant (Martin, Fig. 2), Martin does not describe input relaxation variables, nor output relaxation variables as claimed by applicants in claim 1.

Similarly, Shah fails to describe the above-identified features of claim 1. Shah provides a method for computer-aided design of a product or process. (Shah, title) Although Shah discloses

the use of a plant, and a controller for such plant (Shah, Fig. 1), Shah does not describe the use of input relaxation variables, nor output relaxation variables as claimed by applicants in claim 1.

Because neither Kazmierski, Martin, nor Shah describe, "*mixing a reference input signal and an error signal to generate non-relaxed variables, converting the non-relaxed variables into input relaxation variables through waveform relaxation, processing the input relaxation variables with a high fidelity plant model, generating non-relaxed output variables with the high fidelity plant model, converting the non-relaxed output variables into output relaxation variables through waveform relaxation, and providing the output relaxation variables to a low order controller that generates the error signal*" as taught by applicants' claim 1, applicants respectfully submit that claim 1 and claims 2-14 which depend from claim 1 are not unpatentable under 35 U.S.C. §103(a) over Kazmierski in view of either Martin, or Shah.

The Examiner also rejected claims 15-28 under 35 U.S.C. §103(a) for the reasons set forth in the rejection of claim 1. Claim 15 discloses substantially similar features as claim 1, and recites "*mixing a reference input signal and an error signal to generate non-relaxed variables, converting the non-relaxed variables into input relaxation variables through waveform relaxation, processing the input relaxation variables with a high fidelity plant model, generating non-relaxed output variables with the high fidelity plant model, converting the non-relaxed output variables into output relaxation variables through waveform relaxation, and providing the output relaxation variables to a low order controller that generates the error signal.*" (Emphasis added) Because, neither Kazmierski, Martin, nor Shah disclose these features as taught by applicants for the reasons discussed above with regard to claim 1, applicants respectfully submit that claim 15, and claims 16-28 that depend from claim 15, are not unpatentable under 35 U.S.C. §103(a) over Kazmierski in view of either Martin, or Shah.

The Examiner also rejected claims 29-42 under 35 U.S.C. §103(a) for the reasons set forth in the rejection of claim 1. Claim 15 discloses substantially similar features as claim 1, and recites "*means for mixing a reference input signal and an error signal to generate non-relaxed*

variables, means for converting the non-relaxed variables into input relaxation variables through waveform relaxation, means for processing the input relaxation variables with a high fidelity plant model, means for generating non-relaxed output variables with the high fidelity plant model, means for converting the non-relaxed output variables into output relaxation variables through waveform relaxation, and means for providing the output relaxation variables to a low order controller that generates the error signal." (Emphasis added) Because, neither Kazmierski, Martin, nor Shah disclose these features as taught by applicants for the reasons discussed above with regard to claim 1, applicants respectfully submit that claim 29, and claims 30-42 that depend from claim 29, are not unpatentable under 35 U.S.C. §103(a) over Kazmierski in view of either Martin, or Shah.

For the foregoing reasons, applicant respectfully submits that the applicable objections and rejections have been overcome and that the claims are in condition for allowance. If there are any additional charges, please charge them to our Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Date: April 26th, 2004 Sanjeet Dutta

Sanjeet K. Dutta
Reg. No. 46,145

12400 Wilshire Blvd.
Seventh Floor
Los Angeles, CA 90025
(408) 947-8200